**Laboratory Report Cover Sheet**

**18ECE206J ADVANCED DIGITAL SYSTEMS DESIGN**

**Fourth Semester, 2021-22 (Even semester)**

SRM Institute of Science and Technology College of Engineering and Technology

Department of Electronics and Communication Engineering

**Name :**

**Register No. :**

**Day/ Session :**

**Venue :**

**Title of Experiment :**

**Date of Conduction :**

**Date of Submission :**

|  |  |  |
| --- | --- | --- |
| **Particulars** | **Max. Marks** | **Marks**  **Obtained** |
| Pre lab and Post lab | 10 |  |
| Lab Performance | 20 |  |
| Simulation and results | 10 |  |
| Total | 40 |  |

**REPORT VERIFICATION**

**Staff Name : Signature :**

**7. Implementation of 4 Bit Ripple Carry Adder**

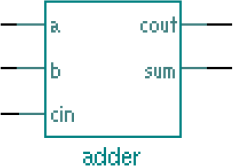
**Aim:** To design and implement 4 Bit ripple carry adder using 4 full adders in VHDL.

**Software Required:**

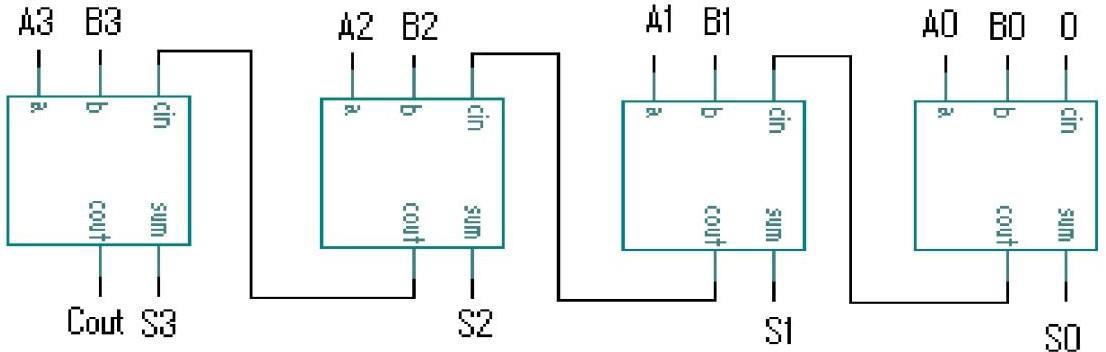
Xilinx ise & ModelSim

#### Theory:

A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. Ripple Carry Adder adds 2 n-bit number plus carry input and gives n-bit sum and a carry output. The Main operation of Ripple Carry Adder is it ripple the each carry output to carry input of next single bit addition. The 4-bit Ripple Carry Adder VHDL Code can be Easily Constructed by Port Mapping 4 Full Adder.



**Fig 1: Full adder block diagram**.



**Fig. 2 Structural description of 4-bit RCA using four full adders**.

**VHDL Code for 4 Bit Ripple Carry Adder:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity Ripple\_Adder is

Port ( A : in STD\_LOGIC\_VECTOR (3 downto 0); B : in STD\_LOGIC\_VECTOR (3 downto 0);

Cin : in STD\_LOGIC;

S : out STD\_LOGIC\_VECTOR (3 downto 0); Cout : out STD\_LOGIC);

end Ripple\_Adder;

architecture Behavioral of Ripple\_Adder is

-- Full Adder VHDL Code Component Decalaration component full\_adder\_vhdl\_code

Port ( A : in STD\_LOGIC; B : in STD\_LOGIC;

Cin : in STD\_LOGIC; S : out STD\_LOGIC;

Cout : out STD\_LOGIC); end component;

-- Intermediate Carry declaration signal c1,c2,c3: STD\_LOGIC; begin

-- Port Mapping Full Adder 4 times

FA1: full\_adder\_vhdl\_code port map( A(0), B(0), Cin, S(0), c1); FA2: full\_adder\_vhdl\_code port map( A(1), B(1), c1, S(1), c2); FA3: full\_adder\_vhdl\_code port map( A(2), B(2), c2, S(2), c3); FA4: full\_adder\_vhdl\_code port map( A(3), B(3), c3, S(3), Cout); end Behavioral;

**Pre-lab questions**

1. What is Ripple adder and its disadvantages?
2. Are Ripple carry adder and binary parallel adder same?
3. Mention the applications of ripple carry adder.
4. What is propagation delay in logic gates? **Post-lab questions**
5. What is the difference between carry look ahead adder and ripple carry adder?
6. What is the gate delay for the 4-bit ripple carry adder?
7. Draw the diagram for 8-bit ripple carry adder.
8. How do you calculate propagation delay? **Result:**